

Application No. : 09/808,469
Filed : March 14, 2001

~~APPENDIX XII~~

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Instruction formats

~~i = instruction opcode~~
~~a = register (r0-3, r13-16)~~
~~b = register (r0-3, r13-16)~~
 5 ~~e = register (r0-3, r13-16)~~
~~h = register high (r0-r31)~~
~~q = condition code~~
~~u = unsigned immediate~~
~~s = signed immediate~~

Op	Format	Instruction	Operands	Comment
0	iiiiqqssssssss	bal/beq/bne	s8	, if cc pc=(pc&0xffffffff)+(s8<<1)
	iiiiilqqssssss	bgt/bge/blt/ble	s6	, if cc pc=(pc&0xffffffff)+(s6<<1)
1	iiisssssssssss	bl	s10	, blink=pc, pc=(pc&0xffffffff)+(s10<<2)
15	2	iiiaaabbbiibii op	a, a, b	, op = sub/and/or/xor/asl/asr/lsl/
			a, b, 1	, asl1/asr1/
			a, b, 2	, asl2/asr2/
			0, a, b	, and.f/mul64/?/?/s_op
		iiiaaaiiil1111 s_op	a, a	, s_op=extb/extw/sexb/sexw/
20			[a]	, j/jl/
			a, a, a	, sub.ne/i_op
		iiiiiil11111111 i_op3		, i_op=brk/j-[blink]/st blink[op,4]/
3	iiiaaaaiuuuuuu	mov/emp	a, u6	
4	iiiaaaaiuuuuuu	add/sub/?/?	a, a, u5	
25	5	iiiaaahhh00hh mov	a, h	
		iiiaaahhh01hh add	a, a, h	
		iiiaaahhhlihh mov/emp	h, a	
6	iiiaaa000iuuu	ld/st	a, [fp, -u3]	, a=mem[fp - (u3 << 2)]
		iiiaaa001iuuu	add/?	a, [fp, -u3], a=fp - (u3 << 2)
30		iiiaaaaiuuuuuu asl/asr/lsl	a, a, u5	
7	iiiaaabbuuuuu	ld	a, [b, u4]	, a=mem[b + (u4<<2)]
8	iiiaaabbuuuuu	ldb	a, [b, u4]	, a=mem[b + u4]
9	iiiaaabbuuuuu	ldw	a, [b, u4]	, a=mem[b + (u4<<1)]
A	iiiaaabbuuuuu	st	a, [b, u4]	, a=mem[b + (u4<<2)]
35	B	iiiaaabb0uuu stb	a, [b, u3]	, a=mem[b + u3]
		iiiaaabbbluuu stw	a, [b, u3]	, a=mem[b + (u3<<1)]
C	iiiaaabbbiuuu	add/sub	a, b, u3	, a=b op u3
D	iiiaaauiuuuuuu	ld	a, [pc, u7]	, a=mem[(pc&0xffffffff)+(u7 << 2)]
E	iiiaaauiuuuuuu	ld	a, [gp, u7]	, a=mem[gp + (u7 << 2)]
40	F	iiiiixxxxxxx reserved		
Other possible formats:				
	iiiaaabb0ccc	ld	a, [b, c]	, a=mem[b + c]
	iiiaaabb1ccc	add	a, b, c	, a=b+c
45		iiiaaauiuuuuuu	add	a, pc, u7, a=(pc&0xffffffff)+(u7 << 2)